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10/603,776	06/26/2003	Luc Burgun	02935.000001.	4879

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EXAMINER	
ALHIJA, SAIF A	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 05/03/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,776	BURGUN ET AL.	
	Examiner	Art Unit	
	Saif A. Alhija	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-25 have been presented for examination.

PRIORITY

2. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in France on 26 June 2002. It is noted, however, that applicant has not filed a certified copy of the 0207949 application as required by 35 U.S.C. 119(b).

Appropriate correction is required.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on **9 July 2004** is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Specification Objections

4. The disclosure is objected to because of the following informalities:

The Specification does not contain labels referring to the Background, Detailed Description, etc. See MPEP 608.01. It appears that the Detailed Description of the invention begins on Paragraph 22 and the Examiner will operate under this assumption.

Appropriate correction is required.

Claim Objections

5. **Claims 1-25 are objected** to because of the following informalities:

i) Claims 1-25 do not separate the preamble from the claim. The claims do not comport to proper U.S. practice.

ii) Claims 21-25 are objected to because it is unclear to which statutory category the claims belong. They appear to recite an apparatus in the form of an Electronic Card.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

MPEP 2106 recites:

The claimed invention as a whole must accomplish a practical application. That is, it must produce a "useful, concrete and tangible result" State Street 149 F.3d at 1373, 47 USPQ2d at 1601-02.

6. Claims 1-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

i) Claims 1-20 discuss a method and system of emulating a design under test, however the claims do not produce a useful, concrete and tangible result since the claims refer only to a connection between two hardware parts rather than, for example, an actual emulating implementation.

ii) Claims 9 and 21 recite an intended use. An intended use is not given patentable weight since an intention is not considered a limitation. Therefore the claim is rendered non-statutory because it does not produce a useful, concrete, and tangible result.

iii) Claims 9, 10, 11, 15, 21, 22, 23, and 25 recite the phrase "capable of". The phrase "capable of" is not given patentable weight since a mere capability is not considered a limitation. Therefore the claim is rendered non-statutory because it does not produce a useful, concrete, and tangible result.

All claims dependent upon a rejected base claim are rejected by virtue of their dependency.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. **Claims 1-25 are rejected** under 35 U.S.C. 102(e) as being clearly anticipated by **Lin et al. "Coverification System and Method", U.S. Patent No. 6,389,379,** hereafter referred to as **Lin.**

Regarding Claim 1:

Lin discloses Method of emulating a design under test associated with a test environment, characterized in that it comprises two distinct generating phases comprising a first phase of generating (80) a first file (FCH1) for configuring the test environment, and a second phase of generating (81) a second file (FCH2) for configuring at least a part of the design under test, the delivery of the first configuration file to a first reconfigurable hardware part (BTR) forming a reconfigurable test bench so as to configure the test bench, and the delivery of the second configuration file to a second reconfigurable hardware part (EML) so as to configure an emulator of the design under test, the two hardware parts being distinct and mutually connected. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 2:

Lin discloses Method according to claim 1, characterized in that the first generating phase (80) comprises the production (800) of a logic circuit (CRL) consisting of a network of logic gates and representative of the test environment as well as of the compilation directives, and a compilation (801) of this logic circuit having regard to the said directives, so as to obtain the first configuration file (FCH1). **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 3:

Lin discloses Method according to claim 2, characterized in that the test environment comprises a collection of drivers (PLi) and of monitors (MNi), and in that the production of the said logic circuit comprises the formation of hardware blocks in the form of networks of logic gates, these hardware blocks representing interfaces of drivers/monitors of software stimulation, interfaces of drivers/monitors of real hardware stimulation, and drivers/monitors of emulated hardware stimulation, blocks for calculations of hardware triggers, as well as a block for interfacing with the emulator of the design under test. **(Figures 28-30 and there corresponding descriptions)**

Regarding Claim 4:

Lin discloses Method according to claim 3, characterized in that the phase of forming the hardware blocks is effected on the basis of statically defined networks of gates or of networks of gates which are generated dynamically by a software module. **(Column 8, Line 21 – Column 9, Line 19)**

Regarding Claim 5:

Lin discloses Method according to any one of claims 1 to 4, characterized in that the first generating phase (80) and the second generating phase (81) are performed in parallel. **(Abstract. Figures**

1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)

Regarding Claim 6:

Lin discloses Method according to any one of claims 1 to 4, characterized in that the first generating phase (80) and the second generating phase (81) are performed sequentially. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 7:

Lin discloses Method according to claim 6, characterized in that the first generating phase (80) is performed before or after the second generating phase (81). **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 8:

Lin discloses Method according to claim 3, characterized in that when the first generating phase is performed after the second generating phase, the production of the logic circuit (CRL) uses as input parameters a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, and in that when the second generating phase is performed after the first generating phase, the production of the logic circuit uses as input parameters a description of the interface of the design under test and supplies as output a description of the assignment of the logic inputs/outputs of the design under test to the pins of the emulator, this output description then being a constraint parameter for the second generating phase. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 9:

Lin discloses Emulation system, intended to emulate a design under test associated with a test environment, characterized in that it comprises a reconfigurable hardware test bench (BTR) capable of emulating a part at least of the test environment, this test bench being connected between a host computer and a reconfigurable hardware emulator (EML), distinct from the test bench, and capable of emulating at least a part of the design under test, first generating means able to generate a first file for configuring the test environment, and second generating means able to generate a second file for configuring the design under test. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 10:

Lin discloses System according to claim 9, characterized in that the reconfigurable test bench (BTR) comprises a so-called fixed part and at least one reconfigurable interface circuit (CRFG) capable of embodying the emulated part of the test environment. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 11:

Lin discloses System according to claim 10, characterized in that the fixed part comprises at least one control circuit (CCTL) and one circuit (CIBS) for interfacing with the host computer, and in that the reconfigurable interface circuit is able to comprise at least interfaces of drivers/monitors of software stimulation which are capable of establishing a communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation. **(Figures 28-30 and there corresponding descriptions)**

Regarding Claim 12:

Lin discloses System according to claim 11, characterized in that the fixed part furthermore comprises additional real hardware drivers/monitors, and in that the reconfigurable circuit (CRFG) is able furthermore to comprise interfaces with these additional real hardware drivers/monitors. **(Figures 28-30 and there corresponding descriptions)**

Regarding Claim 13:

Lin discloses System according to any one of claims 9 to 12, characterized in that the fixed part furthermore comprises a circuit (IFSC) for interfacing with a target device (SYC). **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 14:

Lin discloses System according to claim 9, characterized in that the fixed part furthermore comprises the control part of a hardware logic analyser (AL) whose state evolves as a function of the hardware triggers. **(Column 9, Line 33-58)**

Regarding Claim 15:

Lin discloses System according to claim 9, characterized in that the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals synchronizing the emulator of the design under test and certain at least of the hardware means of the test bench, as well as clock retrocontrol means capable in response to at least one wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary

clock signal of temporarily disabling certain of the other secondary clock signals with different frequencies from that of the first secondary clock signal. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 16:

Lin discloses System according to claim 9, characterized in that the test bench and the emulator are embodied on an electronic card external to the host computer and connected to the latter's mother card. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 17:

Lin discloses System according to claim 9, characterized in that the reconfigurable test bench is embodied on a first electronic card external to the host computer and connected to the latter's mother card, and in that the emulator of the design under test is embodied on one or more other cards external to the host computer and connected to the said first external card. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 18:

Lin discloses System according to claim 17, characterized in that the circuit for interfacing with the target device is integrated into the said first external card. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 19:

Lin discloses System according to any one of claims 10 to 12, characterized in that the test bench and the emulator are embodied on an internal electronic card (CINT) incorporated into the host computer. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 20:

Lin discloses System according to claim 13, characterized in that the circuit for interfacing with the target device is embodied on an external electronic card (CXT) outside the host computer, and able to be connected to the said internal electronic card (CINT). **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 21:

Lin discloses Electronic card, intended to be connected to the mother card of a host computer, characterized in that it comprises a reconfigurable hardware test bench (BTR) capable of emulating a part at least of a test environment associated with a design under test, and a reconfigurable hardware emulator (EML), distinct from the test bench, connected to the reconfigurable test bench and capable of emulating at least a part of the design under test. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 22:

Lin discloses Card according to claim 21, characterized in that the reconfigurable test bench (BTR) comprises a so-called fixed part and at least one reconfigurable circuit capable of embodying the emulated part of the test environment. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Regarding Claim 23:

Lin discloses Card according to claim 22, characterized in that the fixed part comprises at least one control circuit (CCTL) and one circuit for interfacing with the host computer, and in that the reconfigurable circuit is able to comprise at least interfaces of drivers/monitors of software stimulation which are capable of establishing a communication with at least one software process executed on the host computer, and drivers/monitors of emulated hardware stimulation. **(Figures 28-30 and there corresponding descriptions)**

Regarding Claim 24:

Lin discloses Card according to claim 23, characterized in that the fixed part furthermore comprises additional real hardware drivers/monitors, and in that the reconfigurable circuit is able to comprise further interfaces with these additional real hardware drivers/monitors. **(Figures 28-30 and there corresponding descriptions)**

Regarding Claim 25:

Lin discloses Card according to any one of claims 21 to 24, characterized in that the reconfigurable test bench comprises a clock signals generator synchronized by a base system clock and delivering various secondary clock signals of different frequencies, as well as clock retrocontrol means capable in response to a wait signal transmitted by one of the hardware means of the test bench regulated by a first secondary clock signal of temporarily disabling the secondary clock signals with different frequencies from that of the first secondary clock signal. **(Abstract. Figures 1-6, 10 and 16, for example, and there corresponding descriptions. Column 27, Line 45 – Column 28, Line 57)**

Conclusion

8. All Claims are rejected.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saif A. Alhija whose telephone number is (571) 272-8635. The examiner can normally be reached on M-F, 11:00-7:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAA

April 24, 2006

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